Our last issue of 2016 focuses on seven excellent papers in the test field solicited from the 2015 International Test Conference (ITC'15). The goal of the article by Acero et al. is to reduce deterministic test pattern counts in DFT by introducing a new class of test points. The article by Ishida and Ichiyama describes an ATE system that has been evaluated by means of a prototype circuit with a 2.4-GHz QAM signal. The problem of early lifetime defects in interconnects is addressed in the article by Huang et al., where a versatile transition time monitor with low overhead is proposed. The problems associated with manufacturing test of embedded memories with respect to delay faults are described by Ockunzzi et al., who discuss the challenges and provide some novel design-for-test changes in a 32-nm design. Next, Sunter et al. describe how an efficient streaming access can be accomplished and automated by a new command compatible with the IEEE 1687 procedural description language. Then, Barragan et al. target problems associated with test techniques in mixed-signal circuits by means of a practical simulation flow that is capable of evaluating alternative test approaches during their design phase in a fast manner. Finally, Singh et al. introduce symbolic quick error detection as a means to automatically localize and detect logic bugs during postsilicon validation.

In addition to the Special Issue papers, we have four General Interest papers. First, Chang et al. address the problem of handling X ("don't-cares") that is currently not handled in a scalable fashion when dealing with complex circuits. The authors therefore propose a new X-analysis methodology. In the article by Tunaboylu, a new model for power delivery allowing for a 38% reduction in voltage fluctuations is presented. Next, Zaidi et al. evaluate the error performance by means of an FPGA emulator and propose a novel algebraic QC-LDPC code. Finally, Rahimi et al. focus on approximate computing to improve energy efficiency by reusing results of instructions across different processing cores.

In our Departments, we included a Conference Report by Raghunathan and Kellah on the 2016 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED 2016), held in August in San Francisco, CA, and The Last Byte titled “ITC and the Future of Test—We’ve Won” by Press and Wang. Last but not least, we have a novelty regarding our cover design: An illustration by Misha Temkin, a DAC’16 Art Show winner, is shown. The figure is also included inside the issue under the “Silicon Artwork” Department. Special thanks to our editor Sharon Hu who made this possible.

I would like to thank all who contributed to this last issue of 2016 with special thanks going to the Guest Editors Nicola Nicolici and Haralampos-G. Stratigopoulos. Enjoy reading this issue and contact me at henkel@kit.edu for any questions, ideas, or inspirations you may have for future IEEE Design&Test content.

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Editor-in-Chief
IEEE Design&Test