The focus of this issue of IEEE Design & Test (D&T) is on merging memories and is brought to us by Yiran Chen, Tei-Wei Kuo, and Barbara de Salvo. Emerging memory technologies have significant advantages in some of the typical memory characteristics but fall short in others such that their broad adoption continues to be a challenge. This special issue highlights the most prominent problems and their current solutions. The special issue is accompanied by a comprehensive survey “Recent Technology Advances of Emerging Memories” focusing primarily on phase change memory, spin-transfer torque random access memory, and resistive random access memory, which serves as an introduction to the topic.

Besides the special issue, we have two general interest articles. In “Test Cost Reduction Methodology for InFO Wafer-Level Chip-Scale Package,” K.-L. Wang et al. focus on an emerging packaging technology called fan-out wafer-level chip-scale packaging. Cost-effective probing configurations and procedures are reported that may save as much as 40% of the respective cost according to studies on industrial cases. In “Interdependencies of Degradation Effects and Their Impact on Computing,” H. Amrouch et al. focus on circuits aging and how the underlying mechanisms are related and affect computation in future technology nodes.

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The tutorial by P. Mishra et al. “Post-Silicon Validation in the SoC Era: A Tutorial Introduction” continues the successful series of tutorials in IEEE D&T. Thanks to the authors for this issue’s article.

A highlight in our Departments is a Perspective from K. Chakrabarty on “Quo Vadis Test? The Past, the Present, and the Future: No Longer a Necessary Evil.” The author has not only an excellent overview of the field of test, but he is also a former Editor-in-Chief of IEEE D&T. His Perspective focuses on the development of the test field over the past decades in the first part and draws a picture from current and future test directions in the second part, bridging the gap between working silicon and working systems. He also envisions that there will be even more focus on knowledge discovery and adaptive testing in the future. It is my hope that we can cover these upcoming directions in the test field in a future special issue.

Another highlight is the Roundtable discussion on “Designing Secure Electronics: Challenges From a Hardware Perspective.” The Roundtable was held at last year’s DAC in Austin, TX, USA. Thanks to our Roundtable Editor David Yeh for this article on a hot topic and the other roundtable participants Celia Merzbacher, Donna Dodson, Farinaz Koushanfar, Ruby Lee, and Claire Vishik.

A report of the 22nd Asia and South-Pacific Design Automation Conference held in January in Chiba, Japan, is brought to us by Naofumi Takagi.
Scott Davidson, our Reviews Editor, has read the book *Cyber-Physical System Design With Sensor Networking Technologies* and provided a review that is included in this issue. His conclusion reads “…I got a lot more out of this book than I expected to.” This is definitely a good motivation for others interested in the topic to have a look at it as well.

Last but not least, this special issue closes with *The Last Byte* from Scott Davidson with thoughts on “being connected.”

Thanks to all who have contributed to this issue of *IEEE D&T*. If you have any questions or ideas, please contact me at henkel@kit.edu.

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