From the EIC

Verification and Test

This issue is focused on the special issue on “Emerging Challenges and Solutions in SoC Verification” from Guest Editors Magdy Abadir, Jayanta Bhadra, Wen Chen, and Li-C Wang. This special issue on verification is very timely, as new developments demand new verification techniques. For instance, the increasing heterogeneity of on-chip-systems (mainly to increase the power end energy efficiency; see also IEEE Design&Test issue on Dark Silicon, http://ieeexplore.ieee.org/xpl/istocresult.jsp?isnumber=7862860&punumber=6221038) makes verification more complex. Also, the newest trends in application, such as Internet-of-Things, require new verification approaches. The guest editors also present an article on “Challenges and Trends in Modern SoC Design Verification” to round up this interesting special issue. Many thanks to our guest editors for bringing the newest developments to IEEE Design&Test.

For the first time, we have a keynote paper. This new category contains papers that are particularly highlighted to reflect the importance of the topic, the quality of the technical content, etc. Although they are typically invited, any author may submit a keynote paper if it meets the criteria. This first keynote paper is from Huanyu Wang, Qihang Shi, Domenic Forte, and Mark M. Tehranipoor on “Probing Attacks on Integrated Circuits: Challenges and Research Opportunities” and describes invasive physical attacks against security-critical integrated circuits in the form of an overview and open research questions.

We have one general interest paper in the technical paper section. In “Tackling Test Challenges for Interposer-Based 2.5D Integrated Circuits,” Ran Wang and Krishnendu Chakrabarty describe the challenges in test in interposer-based 2.5D circuits among them high power consumption, reduced number of test pins, etc.

Continuing our interview series, our Interview Editor Yao-Wen Chang has taken an interview with Prof. Chenming Hu, the inventor of 3D transistors, who received the National Technology and Innovation Medal from President Obama at the White House in 2016 for his inventions. The interview was held at a conference in Taiwan, where the audience contributed interview questions.

Another highlight from our departments is the visionary perspective article, “Will Chips of the Future Learn How to Feel Pain and Cure Themselves?” This is indeed a very interesting question and this trend might change the way future chips will be designed to sustain reliability. The authors Francky Catthoor and Guido Groeseneken from IMEC give us an inside look from the software and hardware perspective.

Scott Davidson provided a book review entitled “Engineering Secure Internet of Things Systems” on the hot topic of IoT and “The Last Byte.”

Many thanks to all who have contributed to this issue of IEEE Design&Test. If you have any questions or ideas, please contact me at henkel@kit.edu.

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