**Key enabler: Modular Special Instructions (SIs)**

- Problem in state-of-the-art Reconfigurable Processors: Monolithic SIs
  - Our Approach: Reduced reconfiguration overhead but still fast execution due to SI upgrades
  - Example SI for H.264 Motion Estimation: Sum of Abs. Hadamard-Transformed Differences: SATD

**Hierarchical Composition for modular SIs: SIs, Molecules, Atoms**

- Problem: Increased Parallelism implies larger reconfiguration overhead
  - Rotation Manager: Our Novel Run-Time System

**Hardware Implementation: Atom Framework and FPGA Prototype**

Prototyping with a Virtex-4 LX 160, using a Board from Silica/Avnet with Further Peripherals (Video etc.)

**Atom Framework: Infrastructure for Atom Computation and Communication:**

Extending a GPP Pipeline towards RISPP

**Main Contributions**

1. Solved the problem “Parallelism vs. Reconfiguration Overhead”. We can provide both by upgrading the SIs
2. Achieving noticeably better performance than state-of-the-art (see right box)
3. Providing very high adaptivity that is demanded for changing control flow or changing multi-tasking environments

**Results and Conclusions**

- Performance Results and Comparisons: 26x faster than a GPP (Leon 2) when using 8 Atoms
  - Up to 2.38x faster than state-of-the-art reconfigurable Processors (Molen)
  - Depending on the size of the SIs, up to 7.19x faster than the Proteus reconfigurable processor

**Execution Details:** A timeline that shows the execution of 2 hot spots with their temporary SI performance and how they are upgraded

**RISPP: Selected Publications**