In our lab, with industrial collaboration, we have developed a complete H.264/AVC based video compression system on a mid-range FPGA device. The device is capable of compressing larger than 4K (4894×2752) video dimensions at 25 frames per second. Further, we have successfully integrated 4 independent camera-streams which are fed to the FPGA for simultaneous compression.

Now, our focus is implementing the next-generation of video compression standard, High Efficiency Video Coding (HEVC) on a FPGA device using VHDL. HEVC is recently standardized (7th June, 2013) and has a high potential of replacing the current industry standard, H.264/AVC. Therefore, we are witnessing an increasing trend of HEVC IPs introduced to the market.

Implementation of HEVC on a FPGA is more challenging compared to H.264/AVC. Novel concepts and additional coding tools are added to HEVC workflow which increases the workload of compression.

Focus of this work will be efficient design of the constituent modules of HEVC and integration of the complete HEVC system on a FPGA. We will target to optimize writing the raw-video stream from the camera to the on-chip memory and feeding the video data to the compression modules. The HEVC compression pipeline has multiple constituent modules, which must be balanced and area-optimized. Further, these modules must be efficient enough to sustain the frame rate demands. After processing the complete HEVC pipeline, the output video stream is displayed on the monitor. Thus, the HEVC compression system will take input video stream from camera, processes it and feeds it back to the monitor for display in real time.

Required Skills
- VHDL
- Some C/C++ skills

Additional Skills
- Knowledge of MATLAB is a plus

Acquired Skills
- Knowledge of HEVC video compression standard, FPGA implementations, MATLAB

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