Studienarbeit/Bachelor Thesis

“Area and Energy evaluation of a combined ASIC+FPGA implementation of a reconfigurable processor”

Reconfigurable processors utilize a reconfigurable fabric for accelerating compute-intensive parts of applications. The fabric has dedicated regions called as reconfigurable containers to support dynamic loading of application-specific accelerators at runtime.

The i-Core is a typical reconfigurable processor with a runtime reconfigurable instruction set architecture (ISA). The ISA consists of two parts: the core ISA (cISA) and the instruction set extension (ISE). The cISA forms the static part of the i-Core that is implemented by the CPU pipeline, whereas the ISE is realized as reconfigurable special instructions (SIs) that are implemented on a fine-grained reconfigurable fabric such as an FPGA. Figure shows the static and dynamic part of the i-Core architecture, for prototyping reasons currently everything is implemented on an FPGA. However, actually the static part of the i-Core should be implemented as an ASIC that includes the CPU pipeline, the memory hierarchy (caches etc.), dedicated load/store units and address generation units (that allow SIs to access memory), and the interconnects between all these parts and the reconfigurable containers.

In our research project we want to evaluate the area and energy efficiency of the ASIC (static) + FPGA (dynamic) implementation of the i-Core. The entire HDL code is available and tested on an FPGA prototype.

Goals:
This thesis aims at evaluating the area and energy efficiency of a combined ASIC+FPGA implementation of the i-Core. The static part of the i-Core shall be implemented using CAD tools for an ASIC, which involves synthesizing the HDL design using the available technology specific standard cell libraries. The reconfigurable containers shall be synthesized and implemented on an FPGA using the Xilinx CAD tools.

Required/Beneficial Knowledge:
- VHDL
- ASIC
- FPGA

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