Studienarbeit/Bachelor Thesis

“Design and Implementation of hardware accelerators for Heterogeneous Reconfigurable Processors”

Reconfigurable processors utilize a reconfigurable fabric for accelerating compute-intensive parts of applications. The fabric has dedicated regions called as reconfigurable containers to support dynamic loading of application-specific accelerators at runtime.

The \textit{i-Core} is a typical reconfigurable processor with a runtime reconfigurable instruction set architecture. It uses special instructions (SIs) that are composed out of accelerators that are reconfigured into containers at runtime. The accelerators are implemented using a hardware description language (HDL) and they are synthesized/placed\&routed specifically for the containers. The reconfigurable containers of the \textit{i-Core} are all identical (homogeneous).

In this research project we currently investigate a heterogeneous container structure, i.e., the containers differ in their size, resource type and number of inputs and outputs. This leads to efficient utilization of the fabric area with a significant improvement in performance.

**Goals:**

This thesis aims at design and implementation of hardware accelerators for different benchmark applications (e.g. from the MediaBench suite) on the \textit{i-Core} heterogeneous fabric. The hardware accelerators shall be implemented using VHDL and evaluated on our Xilinx Virtex-7 FPGA platform.

**Required/Beneficial Knowledge:**
- VHDL
- FPGA

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