Reliability models are very computational intense. Billions of transistors in a microprocessor operate at billions of operations per second. However, to estimate reliability, we need to estimate the lifetime of a system, i.e. how the system will look like after 10 years. We need to handle the computational complexity by parallelizing the models.

**Goals:**
- Work on current research topics
- Explore parallelism in reliability models scientifically as well as from a programming perspective

**Potential Thesis Topics (open for discussion!)**
- Improving the performance of state-of-the-art reliability models by employing massive parallelism on graphic cards via OpenCL/CUDA
- Employ moderate parallelism in reliability models via OpenCL for CPUs
- Hardware implementation using FPGA and OpenCL.

**Skills acquired with the Thesis**
- Explore Parallelism in complex programs
- Work in a research environment
- Technical writing

**Skills required for the Thesis**
- Programming skills in C
- **NO** OpenCL/CUDA experience required

**Start Date**
Immediately or within a couple of months.

**Language**
English or German.

**Supervision:**
Dipl. Inform. Victor van Santen
victor.santen@kit.edu
http://ces.itec.kit.edu/~vansanten

Dr.-Ing. Hussam Amrouch
amrouch@kit.edu
http://ces.itec.kit.edu/~amrouch