Bachelor Thesis
Design and Implementation of hardware accelerators for Heterogeneous Reconfigurable Processors

Reconfigurable processors utilize a reconfigurable fabric (FPGAs) for accelerating compute-intensive parts of applications. The fabric has dedicated regions called as reconfigurable containers to support dynamic loading of application-specific accelerators at runtime.

The i-Core is a reconfigurable processor with a runtime reconfigurable instruction set architecture. It uses special instructions (SIs) that are composed of accelerators that are reconfigured into containers at runtime. The accelerators are implemented using a hardware description language (HDL) and they are synthesized/placed&routed specifically for the containers. Currently, the reconfigurable containers of the i-Core are all identical (homogeneous).

In a research project we currently investigate a heterogeneous container structure, i.e., the containers differ in their size, resource type and number of inputs and outputs. This enables to have multiple implementations for each accelerator for the specific reconfigurable container types. These implementations can provide a different tradeoff between resource requirements and latency for composing SIs. Overall, this can lead to a more efficient utilization of the fabric area and a performance improvement.

Goals:
This thesis aims at design and implementation of hardware accelerators for different benchmark applications (e.g., from the MediaBench suite) on the i-Core heterogeneous fabric. The hardware accelerators shall be implemented using VHDL and evaluated on our Xilinx Virtex 7 FPGA platform.

Beneficial Knowledge:
- VHDL Programming
- Processor Architecture

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