Approximate Computing is a modern design paradigm that aims to exploit the inherent resilience to errors in a wide set of applications. By bringing good enough results in applications such as image processing and financial analysis, where a unique or golden answer does not exist. Approximate Computing techniques can improve performance in terms of execution time, area, and power/energy, even by orders of magnitude. This can be done, e.g. skipping non-critical computations at software level, reducing circuit complexity or lowering the operation voltage at hardware level.

Existing research works have proposed the synthesis of combinational and sequential approximate circuits like adders and multipliers. These proposals receive an accurate circuit description and perform architectural modifications (i.e. introduce approximations), while keeping the output values within certain defined constraint, e.g. that approximate outputs do not exceed a specific error value respecting accurate one.

Nevertheless, the current trend in the design of complex circuits is moving up in the abstraction level, and the circuits are synthesized from higher-level specifications. High-level synthesis (HLS) presents the ability to generate register-transfer level (RTL) implementations from functional specifications developed in languages such as C, C++ and SystemC (Fig. 1). Once a RTL is produce, current tools flows can be used to map it to FPGAs or ASICs.

Goal:
The goal of this work is to provide capabilities to an existing HLS tool to generate approximate accelerators for error resilient applications. This would require modifications into the current tool flow to introduce and evaluate potential approximations and guarantee that the quality metrics are within user- and application-defined constraints.

Required Knowledge:
- C/C++ programming
- Verilog/VHDL

Helpful skills (not required but helpful):
- Compiler background

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