Bachelor’s/Master’s Thesis

“Analyzing the Effect of Technology Scaling on Trojan Detection Techniques”

For the maximum deployment and trust building of users, IoT devices must be secure enough both at hardware and software level. Malicious modifications or insertions called Trojans, could be made possible by untrusted vendors or foundries at any stage of the IC development cycle.

Problem:
According to Moore’s law, technology scaling results in the shrinking of transistor size, due to which the number of transistors on chip are increasing significantly. Owing to this scaling, detection of smaller Trojans becomes more difficult by traditional post manufacturing testing. Additionally, functional testing may not work for the Trojans that are triggered under rare conditions and remain inconspicuous. However, the presence of an extra circuit/logic or modification in a circuit may effect power consumption, leakage current, and may cause extra delay in the chip.
Side channel signal analysis has been well studied as one of the possible countermeasures against hardware Trojans. Various techniques have been developed using, power fingerprint, delay fingerprint and temperature for different technology nodes (i.e. 90nm, 45nm etc.).

Goals:
This thesis aims at analyzing the effect of technology scaling on different Trojan detection techniques using different types of Trojans.
For proposed analysis, implementation can be done using any of the available ASIC standard tools (e.g. Design Compiler tool from Synopsys etc.) with different technology node libraries. ModelSim (Altera Quartus) can be used for simulation and Synopsys PrimePower for Power analysis. Master’s students will be required to present a lightweight detection technique that fits the best for modern technologies.

Required Knowledge:
- Computer Architecture, VHDL/Verilog

Helpful knowledge:
- Hardware Security
- Design Tools
- Profiling tools (e.g. PrimePower)

You will learn about:
- IoT Security
- Trojan Insertion
- Trojan detection techniques

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