At the Chair for Embedded Systems, we developed a runtime-reconfigurable System based on the Xilinx Zynq. The Xilinx Zynq is a reconfigurable architecture that combines an ARM multi-core and a reconfigurable fabric (FPGA) on a single System-on-Chip. The reconfigurable fabric can be configured with different types of hardware accelerators at runtime, which enables acceleration of compute-intensive applications.

The application domains for such an architecture are manifold, including computer vision and machine learning. The development of hardware accelerators that target applications of these domains is supported by high-level synthesis tools (HLS, i.e., synthesizing hardware from programming languages like C/C+/OpenCL/…). Xilinx provides, e.g., libraries that accelerate functions of the computer vision library OpenCV and support for the deep learning framework Caffe as part of their “reVISION stack” for responsive reconfigurable vision systems. In the embedded systems domain, e.g., autonomous driving or collaborative robots, these systems are subject to non-functional constraints like adherence to deadlines or running under a limited power budget.

In our research, we design algorithms and architectures that enable effective use of the limited reconfigurable area by multiple applications running concurrently on the system. We investigate how non-functional constraints can be met for a subset of the applications, while “best-effort” applications that are not subject to these constraints can run in parallel to achieve a high utilization of the system. We design worst-case execution time analyses, scheduling approaches and hardware extensions. We also investigate how operating systems (e.g., Linux and FreeRTOS) can interface with and manage runtime-reconfigurable accelerators.

Several opportunities for Bachelor-/Master Theses and HiWi Jobs are available in the context of this project.

Potential topic opportunities are for example:
- Design of hardware accelerators, e.g., for computer vision
- Worst-case execution time as well as schedulability analysis and optimization
- Accelerate machine learning using Xilinx’ “reVISION stack”
- Design a toolflow from High-Level Synthesis (C/C+/OpenCL) to custom reconfigurable architectures
- Realize hardware architectures that provide efficient execution of reconfigurable accelerators (VHDL)
- Extend operating systems (Linux, FreeRTOS) to manage a reconfigurable fabric

Feel free to contact us for more information.

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