Abstract - With complexities of Systems-on-Chip rising almost daily, the design community has been searching for new vision that can handle given complexities with increased productivity and decreased times-to-market. The obvious solution, such as increasing levels of abstraction, introducing variety of IPs or offering new design languages will not solve the problem but only prolong the present status of inefficiency and confusion. What is needed is a drastic change in design methodology for prototyping embedded systems that consist of software and hardware. In order to gain in productivity, we need a new approach that will support efficient synthesis and verification of system software and hardware.

In order to find the solution, we will look first at the system gap between SW and HW designs and derive requirements for the design flow that includes software as well as hardware. In order to enable new FPGA tools for model generation, simulation, synthesis and verification, the design flow has to be well defined with unique model semantics and model transformations corresponding to design decisions made by the designers. We will introduce the concept of model refinement that supports this approach and can serve as an enabler for the extreme make-over of system design and system prototyping with FPGAs. We will support this concept with hard data and finish with a prediction and a roadmap toward the final goal of increasing productivity and reducing time-to-market by several orders of magnitude while reducing expertise level needed for design of embedded systems to the basic design principles only.

Short Bio - Daniel D. Gajski received the Dipl. Ing. and M.S. degrees in Electrical Engineering from the University of Zagreb, Croatia and the Ph.D. degree in Computer and Information Sciences from the University of Pennsylvania, Philadelphia.