Abstract:
Recent advances in VLSI technology are resulting in ever more complex system-on-a-chip (SoC) designs. Reduced time-to-market and low product cost requirements have been placing increased pressure upon designers to shift as much as possible of the system functionality onto a set of available microprocessor cores so as to reduce the hardware cost of the system and achieve faster time-to-market. Yet one of the fundamental difficulties in implementing larger parts of SoC functionality in software is the stringent timing constraints of the critical modules; methods need to be developed for matching such stringent constraints if embedded processor cores are to be widely used. Low-cost, application-specific microarchitecture customizations promise to be an efficient solution to this problem. The basic advantage of microprocessor cores versus ASICs is the intrinsic reconfiguration capability of the processor by means of software. In order to preserve this fundamental advantage, application-specific features added to the microarchitecture need to be implemented as reprogrammable hardware. Post-manufacturing customization capability can thus provide seamless migration to new applications possibly due to late specification changes or market requirements, while delivering superior levels of performance.

In this talk, we outline the incorporation of application specific properties into the processor microarchitecture, thus increasing performance and reducing power consumption. The fundamental approach is the identification of application properties during compile time and their dynamic exploitation during program execution by the processor. The basic characteristic of these properties is that their existence can be statically identifiable by the compiler, and that they can lead to significant improvements in performance when exploiting their behavior dynamically. Such properties may consist of the control structure of the algorithm, the run-time data values and the code manipulating some data structures; for example, an array access, its stride, or its control structure. Microarchitectural features that can be enhanced with such application-specific information include the branch predictor, the cache subsystem, and the processor communication infrastructure; techniques aimed at all three are outlined in this talk.

Date and Location:
Friday, June 29th, 2007, 14:00 pm.
University of Karlsruhe, Building 50.34, Room -101
Bio Prof. Alex Orailoğlu

Alex Orailoğlu received his S.B. Degree cum laude from Harvard University in Applied Mathematics and his M.S. and Ph.D. degrees in Computer Science from the University of Illinois, Urbana-Champaign. Alex Orailoğlu is currently a Professor of Computer Science and Engineering at the University of California, San Diego. His research interests include Embedded Systems and Processors, digital and analog test, fault tolerant computing, Computer-Aided Design, and nanoelectronics.

Professor Orailoğlu serves in the technical, organizing and/or steering committees of the major VLSI Test, Design Automation, Embedded Systems and Computer Architecture conferences and workshops. He is an associate editor of the IEEE Design and Test Magazine of the Journal of Electronic Test: Theory and Applications, of the IEE Digital Systems and Design Journal, and of the Journal of Embedded Computing. He has served as the Technical Program Chair of the 1998 High Level Design Validation and Test (HLDVT) Workshop, as the General Chair of HLDVT’99, as the Technical Program Co-Chair of the 2003 CODES/ISSS (ACM/IEEE Hardware Software Codesign Symposium & ACM/IEEE International System Synthesis Symposium), as the General Chair of CODES+ISSS '04, as the Program Co-Chair of the 18th Symposium on Integrated Circuits and Systems Design (SBCCI 2005), as the Program Chair of the IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NanoArch 2005), as the Program Chair of the Workshop on Application Specific Processors (WASP 2005), and as the Vice Program Co-Chair of the 2004 VLSI Test Symposium and of the 2005 VLSI Test Symposium. He currently serves as the Vice Program Co-Chair of the 2006 VLSI Test Symposium.

Professor Orailoğlu is the founding chair of the Workshop on Application Specific Processors (WASP), and has also served as its General and Program Chair in 2002 and 2003. He is also the founding chair of the IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NanoArch). Dr. Orailoğlu currently serves on more than 20 Program Committees of technical meetings in the areas of VLSI Test, Embedded Systems, Computer Architectures, and Nanoelectronics and also serves on multiple steering committees.

Professor Orailoğlu has served as a member of the IEEE Test Technology Technical Council (TTTC) Executive Committee, as the Vice Chair of TTTC, as the Chair of the Test Technology Education Program group, as the Technical Activities Committee Chair and Planning Co-Chair of TTTC. He currently serves as the Communities Chair of the IEEE Computer Society Technical Activities Board. He is the founding chair of the IEEE Computer Society Task Force on Hardware/Software Codesign. Dr. Orailoğlu has published 200 research articles. Dr. Orailoğlu is a Golden Core member of the IEEE Computer Society.