Design and Optimization of Pulse-Driven Circuit

Prof. Youngsoo Shin  
Seoul National University, Korea  
VLSI Design Technology Laboratory, Korea

Abstract
Pulse is a useful signal medium in designing digital circuits. I will explore three possibilities of using pulse in this talk. The first is a pulsed latch, which is a latch driven by a short pulse; it is faster, tolerates some amount of clock skew, and allows some degree of time borrowing. I will review how pulsed latch can be deployed in ASIC synthesis flow and which CAD problems should be addressed. Pulse can conveniently be used to create a dual edge-triggered flip-flop (DETFF), which is a second topic. Design issues regarding DETFF circuits, including timing analysis and clock gating, are addressed; logic synthesis potential by employing DETFFs is also presented. Finally, I will address the possibility of making power supply to carry period pulses so that clock network design is made easier.

Short Bio
Youngsoo Shin received the Ph.D. degree in electronics engineering from Seoul National University, Korea, in 2000. He worked at the University of Tokyo and IBM Watson Research Center before joining KAIST, Korea, in 2004, where he is currently an Associate Professor. His research interests are general field of CAD, in particular low-power, sequential optimization, high-level synthesis, and programmable logic. He is serving as AE of TCAD and TODAES, and organizing and tp members of many conferences.

Date and Location
Thursday, January, 10th, 10:00  
Room H120 Technologiefabrik