Goals of the Lab

Traditionally, embedded processors are designed at the same time as the software development tools are designed that are targeted to a specific embedded processor architecture.

State-of-the-art ASIP design flows, however, do not require to design both, an architecture and its specific software development tools. Instead, an embedded processor is designed starting from a basic processor core, for example, that is adapted to a certain embedded application via extensible instructions, parameters, inclusion/exclusion of pre-defined blocks etc. Software tools are then automatically derived from this description through what is called retargetability. Simply said, through retargetability existing software tools like compilers etc. can be automatically enhanced/generated in order to reflect diverse architectural features.

Aim of this lab is to teach students (semester >=5):

- The shortened design cycle times when using state-of-the-art ASIP design suites with the capability of retargeting software tools compared to traditional embedded processor design.
- The blurred border between hardware and software: since, for example, extensible instructions are specified in a C-like syntax, software and hardware development are no longer two different disciplines but deeply intertwined. Students need skills from both disciplines.
- The tradeoff between power, performance and area. Since the area-delay-product for a given silicon technology is constant, an improvement in one metric may cause another metric to degrade. This is especially important for embedded system design where this tradeoff is purposely exploited in order to meet the given constraints at minimum costs.

The lab was offered in a first run during WS04/05 at Karlsruhe University.

For further details about designing state-of-the-art ASIPs and of how ASIP design flows might help closing the design productivity gap, see: J. Henkel, "Closing the SoC design gap", IEEE Computer Magazine, Vol. 36, Iss. 9, pp. 119-121, Sep. 2003.