On-Chip DRAM Last Level Cache Policies for Multi-Core Systems
Fazal Hameed, Lars Bauer, Jörg Henkel

Motivation and Problem Definition
Advantages for On-Chip DRAM Cache
- provides high cache capacity to hold large working set sizes of emerging applications
- provides half the latency and 8× bandwidth compared to off-chip memory
- provides 8× capacity benefits compared to equivalent area SRAM cache

- Insufficient Resource Allocation
- do not consider application memory access patterns
- always insert data on a miss that leads to increased contention in the DRAM cache
- High Tag Lookup Latency
- reduced row buffer hit latency (maps consecutive memory blocks to different row buffers)
- always reads the tags from the slower DRAM cache
- accesses an SRAM structure named MissMap cache before DRAM cache access to identify DRAM cache hit/miss

Row Buffer Mapping (RBM) and Tag-Cache

Experimental Results for an 8-core system

Conclusions
- ADIP improves performance by 12% compared to LH-Cache [MICRO’11]
- increases hits by 28.9% compared to LH-Cache (reduces off-chip accesses)
- reduces fills by 51.8% compared to LH-Cache (reduces contention in the DRAM cache)
- RMB-ADIP policy improves performance by 5.1% compared to LH-ADIP
- reduces DRAM cache hit latency via improved row buffer hit rate and reduced tag lookup latency compared to LH-ADIP
- has a higher row buffer hit rate (22.1%) compared to LH-ADIP (1.1%)
- has a lower row buffer hit latency (24 cycles) compared to LH-ADIP (43 cycles)
- RMB-ADIP-TC improves the performance by 5.7% compared to RMB-ADIP
- has a higher row buffer hit latency (24 cycles) compared to RMB-ADIP
- has a lower row buffer hit latency (24 cycles) compared to RMB-ADIP-TC

Publications

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