TSP: Thermal Safe Power - Efficient Power Budgeting for Many-Core Systems in Dark Silicon

Outline

- Introduction and State-of-the-art
- Motivation
- Objective and Contributions
- System Model
- Thermal Safe Power (TSP)
  - For Given Mappings
  - For the Worst-Case Mappings
- Evaluations
- Conclusions
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Introduction

Dark Silicon:

- Up to now: Constant power density between technology nodes.

Tech. Node A

$100 \text{ W}$

$100 \text{ mm}^2$

Tech. Node B

$50 \text{ W}$

$50 \text{ mm}^2$

Scaling

$
1 \frac{W}{\text{mm}^2} = 1 \frac{W}{\text{mm}^2}
$
Introduction

Dark Silicon:
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\[
\frac{100 \text{ W}}{100 \text{ mm}^2} = \frac{100 \text{ W}}{100 \text{ mm}^2}
\]

Tech. Node A
- 100 W
- 100 mm\(^2\)

Tech. Node B
- 50 W
- 50 mm\(^2\)

- Expected: Power density doubles between technology nodes.

\[
\frac{100 \text{ W}}{100 \text{ mm}^2} < \frac{200 \text{ W}}{50 \text{ mm}^2}
\]

Tech. Node A
- 100 W
- 100 mm\(^2\)

Tech. Node B
- 100 W
- 50 mm\(^2\)

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Introduction

Dark Silicon:

- Up to now: Constant power density between technology nodes.

  Tech. Node A
  \[ \frac{100 \text{ W}}{100 \text{ mm}^2} = \frac{1 \text{ W}}{1 \text{ mm}^2} \]

  Tech. Node B
  \[ \frac{50 \text{ W}}{50 \text{ mm}^2} = \frac{1 \text{ W}}{1 \text{ mm}^2} \]

- Expected: Power density doubles between technology nodes.

  Tech. Node A
  \[ \frac{100 \text{ W}}{100 \text{ mm}^2} = \frac{1 \text{ W}}{1 \text{ mm}^2} \]

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Introduction

Dark Silicon:

- Up to now: Constant power density between technology nodes.

\[
\text{Scaling} \quad 1 \frac{W}{mm^2} = 1 \frac{W}{mm^2}
\]

Dark silicon motivates:

- Very efficient power budgets.

- Expected: Power density doubles between technology nodes.
Introduction

Dynamic Thermal Management (DTM):

- Avoids possible overheating of the chip.
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- Avoids possible overheating of the chip.

DTM activation:

- Frequent triggers of aggressive DTM $\rightarrow$ Decrease the performance.

\[ T \ [\degree C] \]

\[ V \ [\text{volts}] \]

\[ \text{Time} \]

\[ \text{Hysteresis time} \]
Introduction

Thermal Design Power (TDP):

- Highest expected power for power intensive applications.
- The chip can consume more power than TDP.
- Should be safe to run the system at TDP.
- Manufacturers recommend to design the cooling solution for TDP.
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State-of-the-art

Power Budget / Power Constraint:

- Abstraction: Not deal directly with temperature.
  - Thermal models of applications depend on *neighbouring* cores.
  - Leakage power depends on the core’s *own* temperature.
State-of-the-art

Power Budget / Power Constraint:

- Abstraction: Not deal directly with temperature.
  - Thermal models of applications depend on *neighbouring* cores.
  - Leakage power depends on the core’s *own* temperature.

- Generally, a power budget is a *single* and *constant* value:
  - For each core (per-core).
  - For the entire chip (per-chip), e.g., TDP.
State-of-the-art

Boosting Techniques:

- Allow power levels above the budget for short time intervals.

- For example:
  - Intel’s Turbo Boost.
  - AMD’s Turbo CORE.
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Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.

Highest Temperature: 80.0°C

(a) 8 active cores
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.

Highest Temperature: 80.0°C  
(a) 8 active cores

Highest Temperature: 73.2°C  
(b) 12 active cores
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.

<table>
<thead>
<tr>
<th>(a) 8 active cores</th>
<th>(b) 12 active cores</th>
<th>(c) 16 active cores</th>
</tr>
</thead>
<tbody>
<tr>
<td>Highest Temperature: 80.0°C</td>
<td>Highest Temperature: 73.2°C</td>
<td>Highest Temperature: 69.5°C</td>
</tr>
<tr>
<td>11.27 W 78.9°C</td>
<td>7.52 W 71.6°C</td>
<td>5.64 W 67.8°C</td>
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<tr>
<td>11.27 W 79.5°C</td>
<td>7.52 W 72.2°C</td>
<td>5.64 W 68.5°C</td>
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<td>11.27 W 77.8°C</td>
<td>7.52 W 71.4°C</td>
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<tr>
<td>7.52 W 72.5°C</td>
<td>7.52 W 72.6°C</td>
<td>5.64 W 69.5°C</td>
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<td>60.9°C</td>
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<td>77.6°C</td>
<td>60.9°C</td>
</tr>
<tr>
<td>59.5°C</td>
<td>59.4°C</td>
<td>58.1°C</td>
</tr>
<tr>
<td>58.1°C</td>
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Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.

Highest Temperature: 80.0°C

(a) 8 active cores
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.

(a) 8 active cores

Highest Temperature: 80.0°C

(b) 6 active cores

Highest Temperature: 86.3°C
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.

(a) 8 active cores

Highest Temperature: 80.0°C

(b) 6 active cores

Highest Temperature: 86.3°C

(c) 4 active cores

Highest Temperature: 98.8°C
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.
Motivational Example

- 16 cores with area 5.3 mm$^2$.
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Power budget: 90 W.
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Budgets: 129 W, 90 W, and 59 W per-chip.
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Budgets: 129 W, 90 W, and 59 W per-chip, and 8 W per-core.
Motivational Example

- 16 cores with area 5.3 mm².
- Threshold temperature for DTM: 80°C.
- Budgets: 129 W, 90 W, and 59 W per-chip, and 8 W per-core.

**Example Conclusions:**

**Single** and **constant** power budgets:
- Thermally unsafe.
- Pessimistic.
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Diagram showing cooling and power levels](image)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
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<tbody>
<tr>
<td>90</td>
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<td>70</td>
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<td>65</td>
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<td>90</td>
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<td>60</td>
<td>120</td>
<td>95</td>
</tr>
<tr>
<td>55</td>
<td>140</td>
<td>100</td>
</tr>
<tr>
<td>50</td>
<td>160</td>
<td>105</td>
</tr>
</tbody>
</table>

Max. Temp.  Total Power

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Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Diagram showing temperature and power over time with a TDP of 59 Watts and 8 active cores.](image-url)
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Diagram showing 8 active cores with a TDP of 59 Watts and a graph illustrating temperature and power over time.]
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![ON ON ON ON ON ON ON ON]

![Graph showing temperature and power over time]

- T [°C]
- Time [seconds]
- Power [W]

Max. Temp.  
Total Power

2x TDP
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Heatmap Image]

![Graph Image]
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Diagram showing power and temperature over time with 8 active cores.]

T [°C] 90

0 20 40 60 80 100 120 140 160

Time [seconds]
**Motivational Example**

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Diagram showing temperature and power over time](image)

- Time [seconds]
- Power [W]
- T [°C]
- Max. Temp.
- Total Power

![Graph showing temperature and power over time](image)

- 1.7x TDP
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:
Motivational Example

- **Boosting** over a TDP of 59 Watts.

- 8 active cores:

```
ON ON ON
ON ON ON
ON ON
```

---

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Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Diagram showing active cores and temperature over time]

- Graph showing temperature (°C) and time (seconds) with lines indicating max. temp. and total power. TDP marker is indicated on the graph.

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Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Core Status Diagram]

![Graph]

1.7x TDP

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Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

```
ON ON ON
ON ON ON
ON ON
```

![Graph showing TDP and temperature over time](image_url)
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![8 active cores diagram]

![Graph showing temperature and power over time]

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Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Diagram showing active cores]

![Graph showing temperature and power consumption over time]
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Diagram showing 8 active cores with ON states]

![Graph showing temperature and power over time]

- **1.7x TDP**
Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

![Core Configuration]

![Graph]

- T [°C] 90
- Power [W] 150
- Time [seconds] 160
- Max. Temp. [Red]
- Total Power [Blue]

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Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:
**Motivational Example**

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:

**Example Conclusions:**

- **Boosting** techniques:
  - Do not entirely solve the problem.
  - Boosting only during **short time intervals**.
  - Efficient power budget → Execute **indefinitely**.
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Objective

- Achieve **higher system performance**.

- Efficient power budget:
  - **Thermally safe**: TSP does no trigger DTM.
  - **Not pessimistic**: Allows power values that result in highest temperatures near $T_{DTM}$. 
Objective

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⇒ **Thermal Safe Power (TSP)**
Our Contributions

1. TSP: Given mappings of active cores
   - Accounts for changes in:
     - Mapping decisions.
     - Ambient temperature.
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(a) Mapping example for 6 cores.
Our Contributions

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(a) Mapping example for 6 cores.
TSP $\rightarrow$ 12.74 W per-core.
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(a) Mapping example for 6 cores.
TSP $\rightarrow$ 12.74 W per-core.

(b) Mapping example for 6 cores.
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(a) Mapping example for 6 cores. TSP → 12.74 W per-core.

(b) Mapping example for 6 cores. TSP → 14.64 W per-core.
Our Contributions

2. TSP: Worst-case mappings with $m$ active cores
   - Most pessimistic (lowest) TSP values.
   - Safe for any $m$ active cores
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TSP table built at design time:

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<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
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Per-core budget

- TSP\textsubscript{worst-cases}
Our Contributions

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Per-core budget

Per-chip budget (Estimated)
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System Model

- Thermal model → RC thermal network:
  - Given architecture.
  - Given cooling solution.

- The temperature on a thermal node depends on:
  - Thermal conductances (hardware parameters).
  - Ambient temperature.
  - Power consumption on every core.

- Leakage power: Applications are profiled at $T_{DTM}$. 
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TSP for Given Mappings

For a given mapping \( Q \):

- All active cores consume \( P_{\text{TSP}}(Q) \rightarrow \text{Highest} \) temperatures.
- The temperature on node \( i \) is:

\[
T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b_{i,j}^{-1} \cdot q_j + P_{\text{core \ inact}} \cdot \sum_{\forall j \in K'} b_{i,j}^{-1} (1 - q_j) + \sum_{j=1}^{N} b_{i,j}^{-1} \left( p_{j \text{blocks}} + T_{\text{amb}} \cdot g_j \right)
\]
TSP for Given Mappings

For a given mapping $Q$:

- All active cores consume $P_{\text{TSP}}(Q) \rightarrow \text{Highest}$ temperatures.
- The temperature on node $i$ is:

$$T_i = P_{\text{equal}}: \sum_{j=1}^{N} b_{i,j}^{-1} q_j + P_{\text{core inact}} \sum_{j \in K'} b_{i,j}^{-1} (1 - q_j) + N \sum_{j=1}^{N} b_{i,j}^{-1} (p_j^{\text{blocks}} + T_{\text{amb}} \cdot g_j)$$

Constant for node $i$
TSP for Given Mappings

For a given mapping $Q$:

- All active cores consume $P_{\text{TSP}}(Q) \rightarrow \text{Highest} \text{ temperatures.}$
- The temperature on node $i$ is:

$$T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b^{-1}_{i,j} \cdot q_j + P_{\text{core inact}} \cdot \sum_{j \in K'} b^{-1}_{i,j} (1 - q_j) + N \sum_{j=1}^{N} b^{-1}_{i,j} \left(p_{j}^{\text{blocks}} + T_{\text{amb}} \cdot g_j\right)$$

- Our algorithm: For every node $i$
  - Set $T_i = T_{\text{DTM}}$.
  - Compute $P_{\text{equal}}$.
  - $P_{\text{TSP}}(Q) \leftarrow \text{Minimum } P_{\text{equal}}$. 

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## TSP for Given Mappings

Example for a given mapping $Q$:

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>Active</td>
<td>Active</td>
<td></td>
</tr>
<tr>
<td>Active</td>
<td>Active</td>
<td>Active</td>
<td></td>
</tr>
</tbody>
</table>

[°C]

80
70
60
50
Example for a given mapping $Q$: $T_1 = 80.0^\circ C \rightarrow P_{\text{equal}} = 41.30 W
\begin{align*}
P_{\text{equal}} & \quad P_{\text{equal}} & \quad P_{\text{equal}} \\
P_{\text{equal}} & \quad P_{\text{equal}} & \quad P_{\text{equal}} \\
\end{align*}

$P_{\text{TSP}}(Q) = 41.30 W$
TSP for Given Mappings

Example for a given mapping $Q$:

$T_2 = 80.0^\circ C \rightarrow P_{\text{equal}} = 40.92 W$

$P_{\text{TSP}}(Q) = 40.92 W$
TSP for Given Mappings

Example for a given mapping $\mathbf{Q}$:

$T_3 = 80.0^\circ C \rightarrow P_{\text{equal}} = 42.08\, W$

$P_{\text{TSP}}(\mathbf{Q}) = 40.92\, W$
Example for a given mapping $Q$: $T_4 = 80.0^\circ C \rightarrow P_{\text{equal}} = 44.83 W$

$P_{\text{TSP}} (Q) = 40.92 W$
TSP for Given Mappings

Example for a given mapping $Q$:

\[ T_5 = 80.0^\circ C \rightarrow P_{\text{equal}} = 33.99\, W \]

\[ P_{\text{TSP}}(Q) = 33.99\, W \]
Example for a given mapping $Q$:

$T_6 = 80.0^\circ C \rightarrow P_{\text{equal}} = 33.11\, W$

$P_{\text{TSP}}(Q) = 33.11\, W$
Example for a given mapping $Q$:

$$T_7 = 80.0^\circ C \rightarrow P_{\text{equal}} = 34.60 \text{W}$$

$$P_{\text{TSP}}(Q) = 33.11 \text{W}$$
TSP for Given Mappings

Example for a given mapping $Q$:

$T_8 = 80.0^\circ \text{C} \rightarrow P_{\text{equal}} = 40.30 \text{W}$

$P_{\text{TSP}} (Q) = 33.11 \text{W}$
Example for a given mapping $Q$: 

$T_9 = 80.0^\circ C \rightarrow P_{\text{equal}} = 13.32 W$

$P_{\text{TSP}}(Q) = 13.32 W$
Example for a given mapping $Q$:

$T_{10} = 80.0^\circ C \rightarrow P_{\text{equal}} = 13.04 W$

$P_{\text{TSP}} (Q) = 13.04 W$
Example for a given mapping $\mathbf{Q}$:

\[ T_{11} = 80.0^\circ C \rightarrow P_{\text{equal}} = 13.62 W \]

\[ P_{\text{TSP}} (\mathbf{Q}) = 13.04 W \]
Example for a given mapping $Q$:

$T_{12} = 80.0^\circ C \rightarrow P_{\text{equal}} = 34.93\, \text{W}$

$P_{\text{TSP}}(Q) = 13.04\, \text{W}$
Example for a given mapping $Q$:

$$T_{13} = 80.0^\circ C \rightarrow P_{\text{equal}} = 13.03 W$$

$$P_{\text{TSP}}(Q) = 13.03 W$$
Example for a given mapping $Q$:

\[ T_{14} = 80.0^\circ C \rightarrow P_{\text{equal}} = 12.74 \text{W} \]

\[ P_{\text{TSP}}(Q) = 12.74 \text{W} \]
**Example for a given mapping Q:**

\[ T_{15} = 80.0^\circ C \rightarrow P_{\text{equal}} = 13.31 \text{W} \]

\[ P_{\text{TSP}}(Q) = 12.74 \text{W} \]
Example for a given mapping $Q$:

$T_{16} = 80.0^\circ C \rightarrow P_{\text{equal}} = 34.22 \text{W}$

$P_{\text{TSP}}(Q) = 12.74 \text{W}$
### TSP for Given Mappings

Example for a given mapping $Q$:

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>55.8 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>55.9 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>55.6 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>54.9 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>58.1 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>58.5 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>57.9 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>56.1 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>58.1 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>58.5 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>57.9 °C</td>
<td>12.74 W</td>
</tr>
<tr>
<td>56.1 °C</td>
<td>12.74 W</td>
</tr>
</tbody>
</table>

$P_{TSP}(Q) = 12.74 W$

Polynomial time complexity
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- Introduction and State-of-the-art
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  - For Given Mappings
  - For the Worst-Case Mappings
- Evaluations
- Conclusions
TSP for the Worst-Case Mappings

- Most pessimistic (lowest) TSP value for \( m \) active cores.
- Any \( m \) cores can **safely** consume up to \( P_{TSP}^{\text{worst}}(m) \).
TSP for the Worst-Case Mappings

- Most pessimistic (lowest) TSP value for $m$ active cores.
- Any $m$ cores can safely consume up to $P_{\text{TSP}}^{\text{worst}}(m)$.

For example, with $P_{\text{TSP}}^{\text{worst}}(4) = 14.67$ W:

![Temperature Grid](image)

Highest Temperature: 76.1°C
TSP for the Worst-Case Mappings

- Most pessimistic (lowest) TSP value for $m$ active cores.
- Any $m$ cores can **safely** consume up to $P_{\text{TSP}}^{\text{worst}} (m)$.

For example, with $P_{\text{TSP}}^{\text{worst}} (4) = 14.67$ W:

Highest Temperature: 76.1°C  
Highest Temperature: 75.4°C
TSP for the Worst-Case Mappings

- Most pessimistic (lowest) TSP value for \( m \) active cores.
- Any \( m \) cores can safely consume up to \( P_{\text{TSP}}^{\text{worst}}(m) \).

For example, with \( P_{\text{TSP}}^{\text{worst}}(4) = 14.67 \text{ W} \):

<table>
<thead>
<tr>
<th>Temperature</th>
<th>14.67 W</th>
<th>14.67 W</th>
<th>14.67 W</th>
</tr>
</thead>
<tbody>
<tr>
<td>°C</td>
<td>76.1</td>
<td>75.7</td>
<td>75.4</td>
</tr>
<tr>
<td>°C</td>
<td>56.3</td>
<td>55.8</td>
<td>55.3</td>
</tr>
<tr>
<td>°C</td>
<td>54.3</td>
<td>55.8</td>
<td>55.3</td>
</tr>
<tr>
<td>°C</td>
<td>53.5</td>
<td>55.3</td>
<td>55.3</td>
</tr>
</tbody>
</table>

Highest Temperature: 76.1°C

<table>
<thead>
<tr>
<th>Temperature</th>
<th>14.67 W</th>
<th>14.67 W</th>
<th>14.67 W</th>
</tr>
</thead>
<tbody>
<tr>
<td>°C</td>
<td>54.9</td>
<td>55.3</td>
<td>54.9</td>
</tr>
<tr>
<td>°C</td>
<td>55.3</td>
<td>55.8</td>
<td>55.3</td>
</tr>
<tr>
<td>°C</td>
<td>55.3</td>
<td>55.8</td>
<td>55.3</td>
</tr>
<tr>
<td>°C</td>
<td>54.9</td>
<td>55.3</td>
<td>55.3</td>
</tr>
</tbody>
</table>

Highest Temperature: 75.4°C

<table>
<thead>
<tr>
<th>Temperature</th>
<th>14.67 W</th>
<th>14.67 W</th>
<th>14.67 W</th>
</tr>
</thead>
<tbody>
<tr>
<td>°C</td>
<td>52.4</td>
<td>52.9</td>
<td>53.2</td>
</tr>
<tr>
<td>°C</td>
<td>52.9</td>
<td>53.2</td>
<td>53.0</td>
</tr>
<tr>
<td>°C</td>
<td>53.2</td>
<td>53.2</td>
<td>53.0</td>
</tr>
<tr>
<td>°C</td>
<td>53.2</td>
<td>53.2</td>
<td>53.0</td>
</tr>
</tbody>
</table>

Highest Temperature: 80.0°C
TSP for the Worst-Case Mappings

For $m$ active cores:

- All active cores consume $P_{\text{TSP}}^{\text{worst}}(m) \rightarrow \text{Highest}$ temperatures.
- The temperature on node $i$ is:

$$T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b^{-1}_{i,j} \cdot q_j + P_{\text{core}}^{\text{inact}} \cdot \sum_{\forall j \in K'} b^{-1}_{i,j} (1 - q_j) + \sum_{j=1}^{N} b^{-1}_{i,j} \left( p_j^{\text{blocks}} + T_{\text{amb}} \cdot g_j \right)$$
TSP for the Worst-Case Mappings

For $m$ active cores:

- All active cores consume $P_{\text{TSP}}^{\text{worst}}(m) \rightarrow \text{Highest}$ temperatures.
- The temperature on node $i$ is:

\[
T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} \left( \text{Depends on the mapping } \gamma_j \right) + \sum_{j=1}^{N} \left( \text{Constant for node } i \right)
\]
TSP for the Worst-Case Mappings

For \( m \) active cores:

- All active cores consume \( P^{\text{worst}}_{\text{TSP}} (m) \) → **Highest** temperatures.
- The temperature on node \( i \) is:

\[
T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b_j \cdot q_j + \sum_{j=1}^{N} \left( \text{blocks} \cdot T_\text{amb} \cdot g_j \right)
\]

- Naive algorithm: Brute force.
TSP for the Worst-Case Mappings

For \( m \) active cores:

- All active cores consume \( P_{TSP}^{\text{worst}}(m) \) → Highest temperatures.
- The temperature on node \( i \) is:

\[
T_i = P_{\text{equal}}: \sum_{j=1}^{N} \left( \sum_{q_j} \text{Depends on the mapping } t_j \right) + \sum_{j=1}^{N} \left( \text{blocks } \sum_{i} (\text{blocks}) \right) \text{Constant for node } i
\]

- Naive algorithm: Brute force.
- Our algorithm: **Polynomial Time** → For every node \( i \)
  - Set \( T_i = T_{\text{DTM}} \).
  - Worst-case mapping for node \( i \) → Compute \( P_{\text{equal}} \).
  - \( P_{TSP}^{\text{worst}}(m) \leftarrow \text{Minimum } P_{\text{equal}} \).
### TSP for the Worst-Case Mappings

Example for 4 active cores:

- \( P_{\text{equal}} \) equal \( 80.0{}^\circ\text{C} \)
- \( P_{\text{equal}} \) equal \( P_{\text{equal}} \)

\[
T_1 = 80.0{}^\circ\text{C} \rightarrow P_{\text{equal}} = 14.77\,\text{W}
\]

\[
P_{\text{TSP}}^{\text{worst}} (4) = 14.77\,\text{W}
\]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_2 = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.67 \text{W} \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67 \text{W} \]
Example for 4 active cores:

\[ T_3 = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.67 \text{W} \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67 \text{W} \]
Example for 4 active cores:

\[
T_4 = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.77\text{W}
\]

\[
P_{\text{worst}}^{\text{TSP}} (4) = 14.67\text{W}
\]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_5 = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.67 W \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67 W \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_6 = 80.0^\circ C \rightarrow P_{\text{equal}} = 15.07\, W \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67\, W \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_7 = 80.0^\circ C \rightarrow P_{\text{equal}} = 15.07\,W \]

\[ P_{\text{worst}}^{\text{TSP}} (4) = 14.67\,W \]
Example for 4 active cores:

\[ T_8 = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.67W \]

\[ P_{\text{TSP}}^{\text{worst}}(4) = 14.67W \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_9 = 80.0°C \rightarrow P_{\text{equal}} = 14.67\,W \]

\[ P_{\text{TSP}}^\text{worst} (4) = 14.67\,W \]
Example for 4 active cores:

\[ T_{10} = 80.0^\circ C \rightarrow P_{\text{equal}} = 15.07 \, W \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67 \, W \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_{11} = 80.0^\circ C \rightarrow P_{\text{equal}} = 15.07 W \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67 W \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_{12} = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.67 \text{W} \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67 \text{W} \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_{13} = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.77 \text{W} \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67 \text{W} \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_{14} = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.67 \, W \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67 \, W \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_{15} = 80.0^\circ C \rightarrow P_{\text{equal}} = 14.67\, W \]

\[ P_{\text{TSP}}^{\text{worst}} (4) = 14.67\, W \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

\[ T_{16} = 80.0^\circ C \rightarrow P_{equal} = 14.77W \]

\[ P_{TSP}^{worst}(4) = 14.67W \]
TSP for the Worst-Case Mappings

Example for 4 active cores:

<table>
<thead>
<tr>
<th></th>
<th>52.4 °C</th>
<th>52.9 °C</th>
<th>53.2 °C</th>
<th>53.0 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>53.2 °C</td>
<td>54.1 °C</td>
<td>55.3 °C</td>
<td>54.3 °C</td>
<td></td>
</tr>
<tr>
<td>54.2 °C</td>
<td>57.0 °C</td>
<td>14.67 W</td>
<td>77.3 °C</td>
<td>57.2 °C</td>
</tr>
<tr>
<td>55.4 °C</td>
<td>14.67 W</td>
<td>14.67 W</td>
<td>14.67 W</td>
<td>78.5 °C</td>
</tr>
</tbody>
</table>

\[ P^\text{worst}_{\text{TSP}} (4) = 14.67 \text{W} \]

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Evaluations: Algorithm Execution Time

- TSP for given mappings algorithm.
- On a desktop computer running at 3.10GHz.
- Different numbers of cores.
- 25000 random mappings for every case.
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- On a desktop computer running at 3.10GHz.
- Different numbers of cores.
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![Graph showing execution time vs. cores in floorplan](
![Graph showing execution time vs. cores in floorplan](

- Execution Time [ms]
- Cores in Floorplan

0.23 ms
Evaluations: Algorithm Execution Time

- TSP for given mappings algorithm.
- On a desktop computer running at 3.10GHz.
- Different numbers of cores.
- 25000 random mappings for every case.

![Graph showing execution time vs cores in floorplan]

- Execution Time [ms]
- Cores in Floorplan
- TSP for given mappings
- 1.78 ms
- 0.23 ms
Evaluations: Setup

- 64 core system:
  - *Out-of-order* Alpha 21264 cores in 22 nm.
  - Area of 9.6mm² → From simulations on *gem5* and *McPAT*.
- Every 4 cores → Shared L2 cache and memory controller:
  - Combined area of 4.7mm².
- Available frequencies: 0.1 GHz, 0.2 GHz, . . . , 4.0 GHz.
- RC thermal network: $B^{-1}$ and $G$ → From *HotSpot*.
- **DTM:**
  - Similar to a mode of Intel Xeon 5100 and Intel Xeon 7500.
  - Temperature exceeds $T_{DTM} = 80^\circ C$ → 67% clock cycles are *gated*.
- $T_{amb} = 45^\circ C$. 
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- **64 core system:**
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- Every 4 cores $\rightarrow$ Shared L2 cache and memory controller:
  - Combined area of 4.7mm$^2$.

- Available frequencies: 0.1 GHz, 0.2 GHz, \ldots, 4.0 GHz.

- RC thermal network: $B^{-1}$ and $G \rightarrow$ From *HotSpot*.

- **DTM:**
  - Similar to a mode of Intel Xeon 5100 and Intel Xeon 7500.
  - Temperature exceeds $T_{DTM} = 80^\circ C \rightarrow$ 67% clock cycles are *gated*.

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  - Similar to a mode of Intel Xeon 5100 and Intel Xeon 7500.
  - Temperature exceeds $T_{DTM} = 80^\circ$C → 67% clock cycles are *gated*.
- $T_{amb} = 45^\circ$C.
Evaluations: Hotspot Configuration

- Chip thickness: 0.15 mm
- Silicon thermal conductivity: $100 \frac{W}{m \cdot K}$
- Silicon specific heat: $1.75 \cdot 10^6 \frac{J}{m^3 \cdot K}$
- Heat spreader: $3 \, cm \times 3 \, cm$, and 1 mm thick
- Heat sink: $6 \, cm \times 6 \, cm$, and 6.9 mm thick
- Heat sink convection capacitance: $140.4 \frac{J}{K}$
- Heat sink convection resistance: $0.1 \frac{K}{W}$
- Heat sink and heat spreader thermal conductivity: $400 \frac{W}{m \cdot K}$
- Heat sink and heat spreader specific heat: $3.55 \cdot 10^6 \frac{J}{m^3 \cdot K}$
- Interface material thickness: 20 um
- Interface material thermal conductivity: $4 \frac{W}{m \cdot K}$
- Interface material specific heat: $4 \cdot 10^6 \frac{J}{m^3 \cdot K}$
Evaluations: Benchmarks

- Parsec benchmark suite:
  - H.264 video encoder.
  - Body Track.
  - Black-Scholes Partial Differential Equation option pricing.
  - Swaptions pricing.

- Threads:
  - 1, 2, 3, and 4 parallel dependent threads.
Evaluations: Power Constraints

![Graph showing power consumption vs. number of active cores for different budget scenarios.]

- **Per-core budget [W]**
  - TSP\text{worst}
  - TSP\text{best}
  - 3.6 W per-core

- **Per-chip budget [W]**
  - 150 W per-chip
  - 225 W per-chip
Evaluations: Power Constraints

**Per-core budget [W]**

- TSP\textsubscript{worst}
- TSP\textsubscript{best}
- 150 W per-chip
- 225 W per-chip
- 3.6 W per-core

**Per-chip budget [W]**

- TSP\textsubscript{worst}
- TSP\textsubscript{best}
- 150 W per-chip
- 225 W per-chip
- 3.6 W per-core
Evaluations: Power Constraints

- **Per-core budget [W]**
  - TSP\textsubscript{worst}
  - TSP\textsubscript{best}
  - 150 W per-chip
  - 225 W per-chip
  - 3.6 W per-core

- **Maximum Temperature [°C]**
  - TSP\textsubscript{worst}
  - TSP\textsubscript{best}
  - 150 W per-chip
  - 225 W per-chip
  - 3.6 W per-core
Evaluations: Power Constraints

Temperature distribution:

- 12 active cores (225 W per-chip).

<table>
<thead>
<tr>
<th>Number of Active Cores</th>
<th>TSP worst</th>
<th>TSP best</th>
</tr>
</thead>
<tbody>
<tr>
<td>150 W per-chip</td>
<td>74.6°C - 77.0°C</td>
<td>75.1°C - 78.9°C</td>
</tr>
<tr>
<td>225 W per-chip</td>
<td>75.3°C - 79.5°C</td>
<td>75.0°C - 78.8°C</td>
</tr>
<tr>
<td>3.6 W per-core</td>
<td>74.2°C - 76.8°C</td>
<td>73.3°C - 74.8°C</td>
</tr>
<tr>
<td>150 W per-chip</td>
<td>72.4°C - 73.1°C</td>
<td>71.4°C - 71.5°C</td>
</tr>
</tbody>
</table>

S. Pagani @ CODES+ISSS, ESWeek, 2014
Evaluations: Power Constraints

Boosting Technique (similar to a mode of Intel Xeon 5100):

- Nominal budget: 150 Watts per-chip.
- Boosting power: 225 Watts per-chip.
- Boosting interval: 0.3 seconds.
- Cool-down time: 1.0 second (at nominal power).

If DTM is triggered at nominal power → no boosting.
Evaluations: Dark Silicon Estimations

Number of Active Cores vs. Per-core budget [W]

- $P_{\text{core min}}$
- TSP\text{worst}
- 150 W per-chip

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Evaluations: Dark Silicon Estimations

\[ P_{\text{core min}} \]

- Number of Active Cores
- Per-core budget [W]

- TSP\textsubscript{worst}
- 150 W per-chip

37 cores
Evaluations: Dark Silicon Estimations

Number of Active Cores vs. Per-core budget [W]

- **TSP\textsubscript{worst}**
- **150 W per-chip**

- 37 cores
- 54 cores

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Evaluations: Dark Silicon Estimations

Percentage:
- $150 \text{ W per-chip} \rightarrow 42\%$ of the chip is dark.
- $\text{TSP}_{\text{worst}} \rightarrow 16\%$ of the chip is dark.

Per-core budget [W]

Number of Active Cores

37 cores

54 cores
Evaluations: Performance

- H.264 video encoder:

![Graph showing performance evaluations for H.264 video encoder with different power consumption scenarios.]

- Giga-Instructions Per Second (GIPS)
- Number of Active Cores: 8, 16, 24, 32, 40, 48, 56, 64
- Power scenarios: 150 W per-chip, 225 W per-chip, 3.6 W per-core, Boost (150 W)

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Evaluations: Performance

H.264 video encoder:

- TSP\textsubscript{worst}
- TSP\textsubscript{best}
Evaluations: Performance

- H.264 video encoder:

![Graph showing performance of H.264 video encoder with number of active cores vs. Giga-Instructions Per Second (GIPS). There are two lines, one labeled TSP_{worst} and the other TSP_{best}. The graph highlights better mapping decisions with an arrow pointing to a section of the graph.]

- TSP_{worst}
- TSP_{best}

Better mapping decisions

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Evaluations: Performance

H.264 video encoder:

- 

\[
\begin{align*}
\text{TSP}_{\text{worst}} & \quad \text{3.6 W per-core}
\end{align*}
\]

Giga-Instructions Per Second (GIPS)

Number of Active Cores

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Evaluations: Performance

- H.264 video encoder:

![Graph showing performance of H.264 video encoder.](image)

- Pessimism of the budget

- Number of Active Cores

- Giga-Instructions Per Second (GIPS)

- $TSP_{\text{worst}}$

- 3.6 W per-core

- 150 W per-chip

- 225 W per-chip

- 3.6 W per-core

- Boost (150 W)

- S. Pagani @ CODES+ISSS, ESWeek, 2014
Evaluations: Performance

H.264 video encoder:

- TSP_{worst}
- 225 W per-chip
Evaluations: Performance

H.264 video encoder:

- TSP\textsubscript{worst}
- 225 W per-chip

Frequent DTM activation

Number of Active Cores

Giga-Instructions Per Second (GIPS)
Evaluations: Performance

- H.264 video encoder:

![Graph showing performance evaluations.](image-url)

- TSP\textsuperscript{worst} (62) = 3.6 W
- All cores run at 2.3 GHz (2.9 W)
Evaluations: Performance

H.264 video encoder:

- A few cores run at 2.3 GHz (2.9 W)
- Most cores run at 2.4 GHz (3.7 W)

Giga-Instructions Per Second (GIPS)

Number of Active Cores

TSP_{\text{worst}} (62) = 3.6 W

All cores run at 2.3 GHz (2.9 W)
Evaluations: Performance

- H.264 video encoder:

![Graph showing performance of H.264 video encoder](image)

- TSP\textsubscript{worst}
- 150 W per-chip

Giga-Instructions Per Second (GIPS)

Number of Active Cores

- 150 W per-chip
- 225 W per-chip
- 3.6 W per-core

S. Pagani @ CODES+ISSS, ESWeek, 2014
Evaluations: Performance

- H.264 video encoder:

![Graph showing performance metrics with TSP\textsubscript{worst} and 150 W per-chip lines.]

- Frequent DTM activation

- 150 W per-chip

- 225 W per-chip

- 3.6 W per-core

S. Pagani @ CODES+ISSS, ESWeek, 2014
Evaluations: Performance

H.264 video encoder:

![Graph showing Giga-Instructions Per Second (GIPS) vs. Number of Active Cores]

- TSP\textsubscript{worst}
- 150 W per-chip

Pessimism of the budget

S. Pagani @ CODES+ISSS, ESWeek, 2014
Evaluations: Performance

H.264 video encoder:

- **TSP\text{worst}**
- **150 W per-chip**
- **Boost (150 W)**

![Graph showing performance of H.264 video encoder](image-url)

Number of Active Cores vs. Giga-Instructions Per Second (GIPS)
Evaluations: Performance

- H.264 video encoder:

  - Frequent DTM activation at nominal power

  ![Graph showing performance metrics for H.264 video encoder]

  - TSP_{worst}
  - 150 W per-chip
  - Boost (150 W)

  - Giga-Instructions Per Second (GIPS)

  - Number of Active Cores

  - 150 W per-chip
  - 225 W per-chip
  - 3.6 W per-core

S. Pagani @ CODES+ISSS, ESWeek, 2014
Evaluations: Performance

H.264 video encoder:

- Boosting is not good enough
Evaluations: Performance

H.264 video encoder:

- TSP_{worst}
- TSP_{best}
- 150 W per-chip
- 225 W per-chip
- 3.6 W per-core
- Boost (150 W)
Evaluations: Performance

(a) x264
(b) Body Track
(c) Black-Scholes
(d) Swaptions

Giga-Instructions Per Second (GIPS)

Number of Active Cores
Evaluations: Performance

TSP\textsubscript{worst} vs. State-of-the-art:

- \textbf{50\% higher performance} compared to all constant power budgets.
- \textbf{14\% higher performance} compared to the \textit{boosting} technique.
Outline

- Introduction and State-of-the-art
- Motivation
- Objective and Contributions
- System Model
- Thermal Safe Power (TSP)
  - For Given Mappings
  - For the Worst-Case Mappings
- Evaluations
- Conclusions
Conclusions

- **Single** and **constant** power budgets:
  - Thermally unsafe.
  - Pessimistic.

- **Boosting** techniques:
  - Do not solve the problem.

- Thermal Safe Power (TSP) $\rightarrow$ **Safe** and **efficient** power budget:
  - Given mappings $\rightarrow$ Online.
  - Worst-case TSP $\rightarrow$ Abstracts from mapping decisions.

- TSP $\rightarrow$ Fundamental new step in dark silicon:
  - Alleviates pessimistic estimations of TDP $\rightarrow$ **Less dark silicon**.
  - Enables **new performance improvements** compared to State-of-the-art.
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Thank you!

Questions?

TSP source-code:
http://ces.itec.kit.edu/download
Thank you!

Questions?

TSP source-code:

http://ces.itec.kit.edu/download
Appendix

- Voltage/Frequency Settings
- Different Power Constraints per Core
- Best-Case Mapping for Uniform TSP
- Transient State Considerations
## Appendix: Voltage/Frequency Settings

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<tr>
<th>Frequency [GHz]</th>
<th>Voltage [V]</th>
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<tr>
<td>0.4</td>
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</tbody>
</table>
Appendix

- Voltage/Frequency Settings
- Different Power Constraints per Core
- Best-Case Mapping for Uniform TSP
- Transient State Considerations
Appendix: Different per-core Budgets

- **Objective:** Maximize the total power consumption for mapping $Q$.
- The problem can be formulated as a *linear programming*:

\[
\text{Maximize} \quad \sum_{i=1}^{N} p_{i}^{\text{cores}}
\]

such that:

\[
BT - P^{\text{cores}} = P^{\text{blocks}} + T_{\text{amb}} G
\]

\[
\sum_{i=1}^{N} p_{i}^{\text{cores}} \leq P_{\text{max}} - \sum_{i=1}^{N} p_{i}^{\text{blocks}}
\]

\[
T_{i} \leq T_{\text{DTM}} \quad \text{for all } i \in K
\]

\[
T_{i} \geq 0 \quad \text{for all } i = 1, 2, \ldots, N
\]

\[
p_{i}^{\text{cores}} = 0 \quad \text{for all } i \notin K'
\]

\[
p_{i}^{\text{cores}} = P_{\text{inact}}^{\text{core}} \quad \text{for all } i \in K' \text{ and } q_{i} = 0
\]

\[
p_{i}^{\text{cores}} \geq P_{\text{min}}^{\text{core}} \quad \text{for all } i \text{ in which } q_{i} = 1.
\]

- **Result:** Vector with a different power constraint for each active core.
Appendix: Different per-core Budgets

Example for 4 active cores:

(a) Total power: 62.2 Watts

(b) Total power: 67.4 Watts
Appendix

- Voltage/Frequency Settings
- Different Power Constraints per Core
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- Transient State Considerations
Appendix: Best-Case Mapping for TSP

- **Objective:** Find the best-case mapping for \( m \) active cores.
- The problem can be formulated as an **integer linear programming**:

  \[
  \text{Maximize } \quad P_{\text{equal}}
  \]

  such that:

  \[
  T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b^{-1}_{i,j} \cdot q_j + P_{\text{core}} \cdot \sum_{\forall j \in K'} b^{-1}_{i,j} (1 - q_j) + \sum_{j=1}^{N} b^{-1}_{i,j} \left( p_j^{\text{blocks}} + T_{\text{amb}} \cdot g_j \right)
  \]

  \[
  T_i \leq T_{\text{DTM}} \quad \text{for all } i \in K
  \]

  \[
  \sum_{j=1}^{N} q_j = m
  \]

  \[
  q_j = 0 \quad \text{for all } j \notin K'
  \]

- **Result:** Vector \( Q \) with the best-case mapping for \( m \) active cores.
Appendix

- Voltage/Frequency Settings
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- Transient State Considerations
Appendix: Transient Considerations

- Consider a 16 chip with TDP = 90 Watts.
- Consider a transition between two steady-states:

(a) 8 active cores: 90 W

(b) 4 active cores: 59 W
Appendix: Transient Considerations

Temperature during transition

\[ 90 \text{ W} = 8 \cdot P_{TSP}^{\text{worst}}(8) = \text{TDP} \]

\[ 59 \text{ W} = 4 \cdot P_{TSP}^{\text{worst}}(4) < \text{TDP} \]
Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 80.0°C
Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 80.0°C

Δ$T_{\text{transient}}^{\text{max}} = 15.08^\circ\text{C}$
Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 65.0°C

\[ \Delta T_{\text{transient}}^{\text{max}} = -6.41°C \]
Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 71.0°C

\[ \Delta T_{\text{transient}}^{\text{max}} = 2.18^\circ\text{C} \]
Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 69.0°C

\[ \Delta T_{\text{max}}^{\text{transient}} = -0.68^\circ C \]
Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 69.5°C